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Widely Configurable, DC Operated UPS for Small and Mid Sized Battery Backup Applications

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Abstract: Today's desired power managing devices are smart, embeddable, highly energy efficient and with small form factor. The paper provides details concerning the design and implementation of a miniature uninterruptible power supply (UPS). The battery charging and balancing is analyzed and practical measurement results are presented. The performance can be raised with optimized control algorithms implemented on a powerful MCU platform capable of performing even multiple tasks in parallel. A good shaped charging and balancing algorithm can increase overall battery lifetime and performance when backing up critical systems that need to be up all the time, and doing all these at a relatively reduced cost. Fast reaction time of the system is critical so that the devices connected to the UPS output remain always powered. Several reconfigurable electrical and environmental parameters and different communication channels with this smart UPS ensure that it can be embedded in a wide range of electrical systems.

Keywords: UPS, battery charging, battery balancing, MCU, control algorithms, balancing algorithm, ADC, PWM, USB, I^2C, FLCS, embedded system.

1. Introduction

An UPS provides electrical power for a home automation system or server center when the main power fails, drawing stored energy from battery cells. With the fast growing number of intelligent electrical devices and computer systems that need to be powered 24h per day, 7 day per week the need arises for intelligent UPS solutions that are highly flexible and which can be easily integrated and embedded in existing solutions. In order to maintain the battery's capacity at maximum rate, the battery's cells need to be balanced periodically.

This means transferring energy from or to individual cells, until the state of charge (SOC) of each individual cell is equal to the battery's overall SOC.

In order to assure great flexibility the UPS should have wide input voltage range, digitally configurable output voltage range, should be able to charge multiple chemistry batteries and it should be able to balance multiple, serially connected cells used in a battery pack in order to maximize the overall capacity and lifetime of the battery.

The main goal of this paper is to present and prove all the methods used to fulfilling these requirements in a smart, embeddable UPS for small and mid size battery backup applications.

2. Levels of integration

Early in 2009 Microchip's engineers elaborated a quick classification guide [11] regarding the intelligent power supply topologies, defining four levels of integration: the lowest level was occupied by the On/Off control, the mid level was reserved for proportional control, at the third level stays the topology control, at the top level resides the full digital control. This classification somehow inspires our main UPS project, maintaining our goal to reach the highest possible level of integration. In order to determine a similar classification for UPS devices we are interested in, we try to reformulate the integration level constraints as follows.

Basic level of UPS integration: On/Off Control

The UPS's logical shell provides limited on/off control functions through a rudimentary, switch or jumpers based "user interface". Startup sequences, shutdown condition and battery fault detection can be set up for a standard analog design. On the basic level of integration the UPS has a deterministic response to system fault events.

Basic level integration does typically involve some monitoring and control functions, all functions coverable by tiny or small class microcontrollers with integrated voltage comparators and ADCs. These devices provide for the UPS a limited intelligence and integration capability by controlling the output sequencing and monitoring of input/output voltage, current and temperature.

Mid level of UPS integration: Proportional Control

This second integration level adds the digital control to the standard analog design. The basic level features remain, but it is possible to set up voltage and current thresholds, control output voltage, and even set up desired thermal limits. At the mid level, most of the operating parameters of the UPS can be digitally controlled and monitored. All these features allow better UPS

environment monitoring. ADC inputs are used to monitor the UPS inputs, batteries and outputs, comparators can also be used to ensure fast response to system events or faults. Digitally controlled PWM generators provide direct control of the analog PWM circuitry of the UPS. The MCU even dedicates communication channels (SPI, I2C, USB) to upper levels of user control. At this level of integration the reliability of the system is determined by the analog SMPS design with the absolute performance specifications determined by the MCU firmware performance.

High level of UPS Integration: Topology Control

At this level the standard analog design at the mid level of integration even the structure of the control loop can be reconfigured changing from a PWM control loop to a hysteretic [15] control loop at light loads. This allows for changing between continuous inductor current mode and discontinuous conduction mode, increasing system efficiency. The MCU runs more advanced control algorithms and also maintains communication channels (SPI, I2C, USB) to upper levels of user control.

Top level of UPS Integration: Digital Control

Full digital control replaces the standard analog UPS design and provides all of the UPS functions supported on lower integration levels. The SMPS-s (charger and main PSU) regulation functions are directly controlled by the digital circuits of the MCU (PWM generators, ADC-s) and by the control algorithm running on the MCU. This is how the full digital solution allows using techniques that are not possible employing only analog solutions. Some proprietary compensation algorithms can be used to maintain batteries at maximum performance level or to recover them if they become slightly damaged. The full digital solution enables customized response to power input change or load change events increasing the system efficiency. The MCU also dedicates communication channels to upper levels of user control offering a wide palette of settings and control parameters.

At this level the UPS can be easily embedded in any digital system, which can lower system cost and increase system efficiency.

3. Detailing the internal architecture

Our developed UPS solution is based on a combination between the High and Top integration levels to achieve optimal results. *Fig. 1* shows a highly flexible, 8 bit, RISC MCU based device with two separate, highly efficient buck-boost converters with digitally adjustable PWM control. Both the Output Buck/Boost block (which acts as the main PSU of the system) and the Charger

Buck/Boost block have their own digital potentiometer involved in their voltage feedback circuit, thus the MCU can directly control output voltage and charging voltage level through them. Low pass filters and external A/D converter are used to provide multi-channel, high resolution, filtered voltage measurements from batteries and input, output rails. A MOSFET based switching matrix is responsible for fast and efficient (with low losses) power path connections inside the system. The connected batteries and the main PCB temperatures are permanently monitored allowing an additional level of security to the system. The MCU also dedicates communication channels (USB and SMBUS) to upper levels of user control offering a wide palette of settings and control parameters to be changed in real time.

In order to minimize switching losses for different combinations of input and output voltages the switching frequency of the buck-boost converters can be set by a PWM signal generated from the MCU. This feature is one of the High level integration properties; the analog SMPS buck-boost outputs are digitally adjustable.

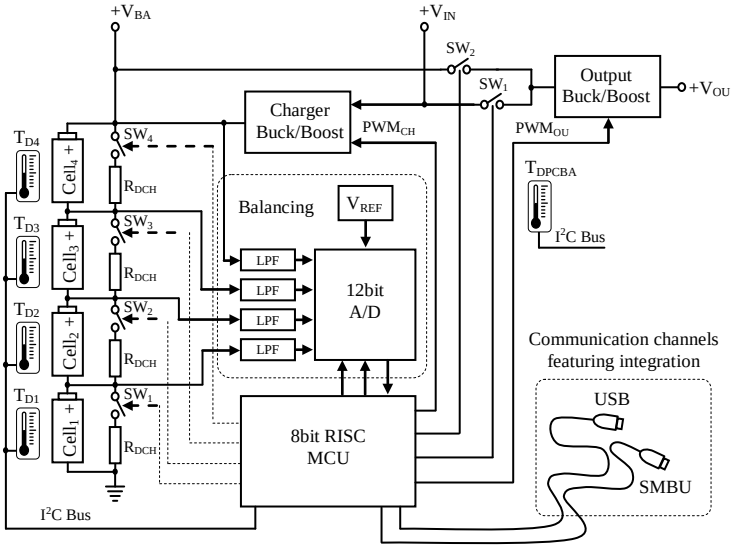

Figure 1: General schematic of the smart, micro-UPS, presenting the most important component blocks inside the device.

3.1. The charging circuit

The design also contains a highly flexible charger which has to work with several battery types and chemistries, therefore the charging voltage and current needs to be digitally fine-tuned on a wide scale. Because the required output charging voltage is often bigger than the maximum allowed voltage supported

by the digital potentiometers, they will be positioned in a low side configuration as it is shown in *Fig. 2*.

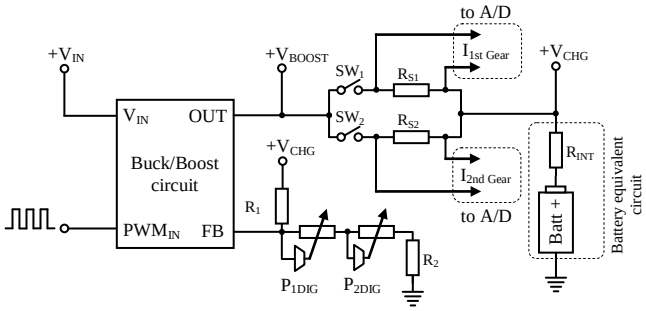

Figure 2: Schematic of the charging circuit.

Since the potentiometers are located on the low side of the voltage feedback circuit, the achieved voltage/current resolution is not linear, so to fulfill the voltage/current resolution requirements we opted for a design with two digital potentiometers with different resistance values and resolution (7bit and 8 bit) in series.

In order to increase the precision of constant current regulation the current steps needs to be small. The charging converter is operated in voltage control mode and the current through the charging resistor is determined by the converter output voltage. Thus, the resolution of the charging current depends on the resolution of the output voltage. In the design two current shunts were used for the possibility to limit high and low currents and for better current regulation and measurement at low charge currents. This helps determining possible end of charge conditions for different battery types. Each of these resistors is in series with a P channel MOSFET switch. The internal resistance of the switch also adds to the overall resistance of the charging circuit. The charging voltage is measured through a separate 12 bit A/D converter.

The charging buck-boost converter's output voltage is expressed by:

$$U_{BST} = U_{FB*}\left(1+\frac{R_1}{R_{P1}+R_{P2}+R_2}\right) \tag{1}$$

Fig. 3 shows the simulation results about the relation between the digital potentiometer P2 settings and the charging buck-boost converter's output voltage at different P1 settings.

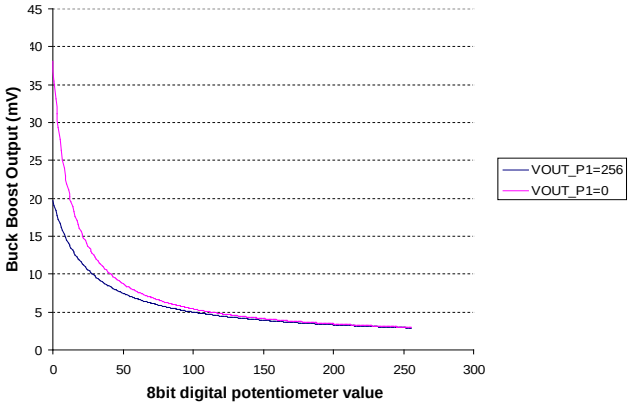

Figure 3: Rough tuning of the Charging Buck-Boost converter output voltage with digital potentiometer P2.

Fig. 4 shows the simulation results about the relation between the digital potentiometer P1 settings and the charging buck-boost converter's output voltage at different P2 settings.

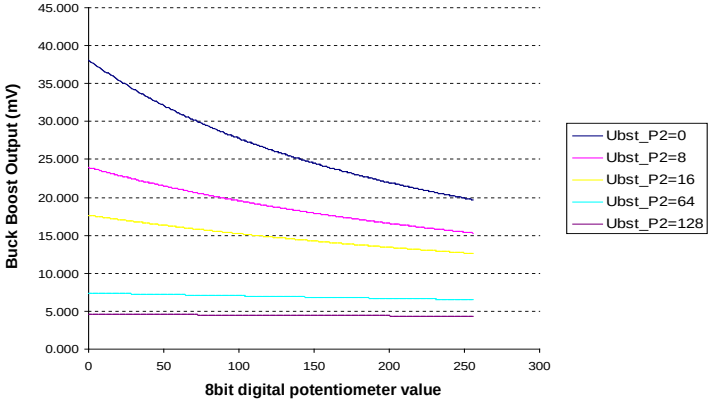

Figure 4: Fine tuning of the Charging Buck-Boost converter output voltage with digital potentiometer P1.

The voltage and current steps are defined by the following equations:

$$U_{step} = U_{BST} - U_{BAT} \tag{2}$$

$$I_{step} = \frac{U_{step}}{R_S + R_{DSon} + R_{INT}} \tag{3}$$

Fig. 5 shows the simulation results about the relation between the digital potentiometer P1 settings and the charging voltage steps at different P2 settings.

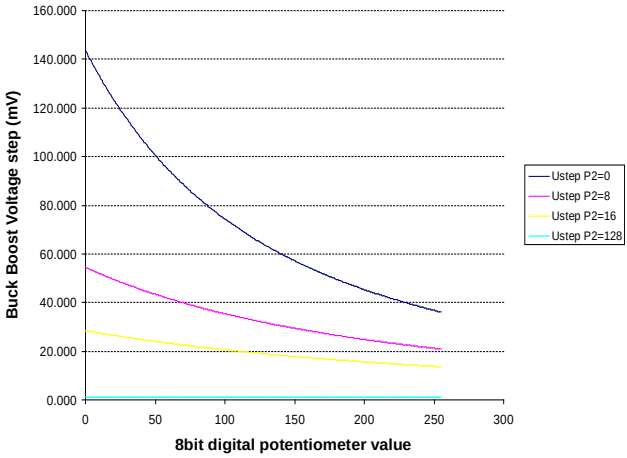

Figure 5: Charge voltage step.

Fig. 6 shows a simulation result about the relation between the control input of the digital potentiometer P1 settings and the charge current steps at different P2 settings.

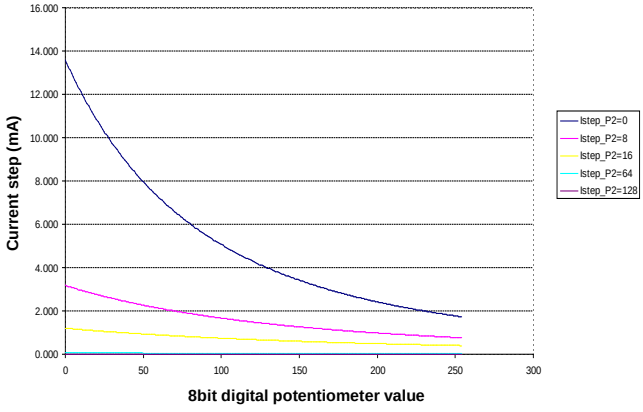

Figure 6: Charging current step variation for R_S=22mΩ, R_{INT}=10mΩ.

If the battery's internal resistance (R_{INT}) is not known or it is changing by battery aging, it can be identified and calculated using equation (4). The charger system applies two different charging voltage levels and measures the voltage on the battery and the charging current.

$$\begin{aligned} U_{CHG1} &= I_{CHG1} * R_{INT} + U_{BAT} \\ U_{CHG2} &= I_{CHG2} * R_{INT} + U_{BAT} \end{aligned} \tag{4}$$

where:

U_{BAT}: is the voltage measured on the battery when the charging current is 0
U_{CHGn}: is the voltage measured on the battery when charging
U_{BST}: is the output voltage of the buck-boost converter

We can quickly find the two unknown values from this equation i.e. the internal resistance and the actual battery voltage. For better results several measurements are made and the arithmetic mean is used for further processing. A simplified technique used in practice is to measure the battery voltage in open circuit (at $I_{CHG1}=0$) which results in the case $U_{CHG1}=U_{BAT}$.

For the battery voltage range from 5V to 30V knowing the internal resistance of the battery helps the charging system to estimate the effect of a voltage step applied to the battery. It has a direct impact on the current step applied to the battery and by knowing this information the precision of the constant current regulation can be greatly improved.

3.2. The charging algorithm

The applied charging algorithm consists of five main steps as follows.

Step 1: Check the battery state – temperature and voltage. If there is no over-voltage or over-temperature the charging process can be started.

Step 2: Pre-charge stage – Switch to low current charging stage by selecting the higher value shunt resistor (R_{S1}). Ramp up fast the charging voltage, until a small amount of charge current is sensed. Limit the current to a small predefined level and keep on charging until the battery voltage exceeds a pre-charge voltage threshold. Proceed forward to Step 3.

Step 3: Constant current stage – Switch to high current charging stage by selecting the lower value shunt resistor (R_{S2}). Ramp up the charge current and limit the current by regulating it to the predefined value. If the battery voltage exceeds the maximum allowed bulk voltage than proceed forward to Step 4.

Step 4: Constant Voltage stage – Apply the bulk voltage to the battery until the charge current drops to a predefined small value than proceed forward to Step 5.

Step 5: Depending on the battery chemistry float charge is applied.

During all stages the charge current is also regulated depending on the temperature of the battery cells and of the PCB. If during charging the battery temperature is above the normal limits the charge current is gradually lowered. If the battery temperature exceeds the maximum allowed threshold the charging is immediately stopped.

The measurements results when charging 3x3400mAh LiFePO4 cells connected in series are presented in *Fig. 7*.

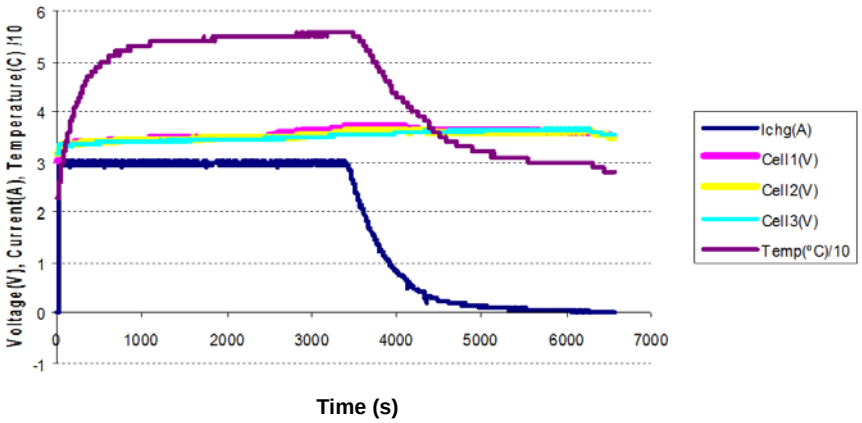

Figure 7: Constant current, constant voltage charging diagram scaled with the temperature response of the board.

3.3. Fuzzy charging control

The proposed Fuzzy Logic Control algorithm is used mainly because robust control is needed, with more than one control rules. If there is an error in one of the measurements the impact of the decision is not fatal. The digital potentiometer used is a cheap one because of economical constrains, but it has also poor precision (20% only) so using a lookup table for possible charge voltages is not possible.

The Fuzzy Logic Control System (FLCS) is presented in *Fig. 8*.

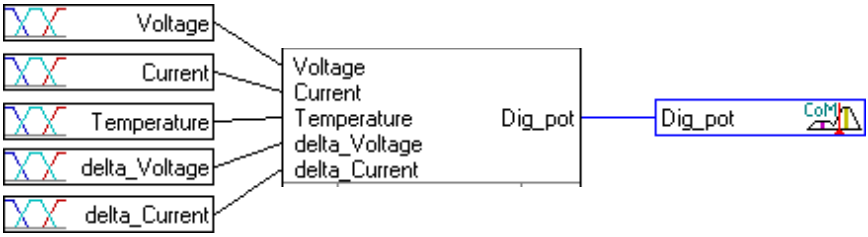

Figure 8: The Fuzzy Logic Control System.

The input variables are defined as: Voltage [5-30V], Current [0-3A], delta_Voltage (difference between the desired battery voltage and current battery voltage), delta_Current (difference between the desired charge current and current charge current), Temperature (battery temperature). The output variable is defined as: Dig_pot (the digital potentiometer value). The charging voltage range is between 0-30V, the desired set voltage is 14.4V. *Fig 9.* shows the charging voltage is not at the desired voltage. Changing the digital potentiometer resistance has a nonlinear, nearly exponential effect on the charging voltage in the upper range of the desired voltage. This had to be accounted for by selecting the Fuzzy membership functions accordingly. *Fig. 10* shows the delta_Voltage, currently at -0.3V.

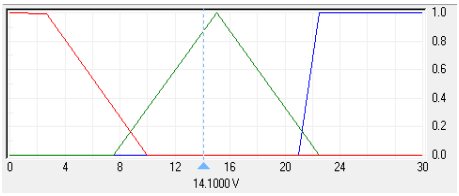

Figure 9: Membership function of the charging voltage input.

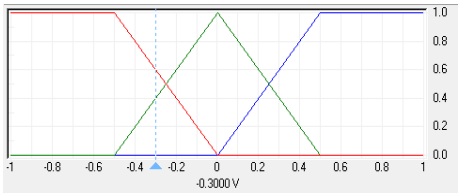

Figure 10: Membership function of the charging voltage error input.

The charging current can vary between 0-3A, the desired current in the presented example is 2A. The charge current information is correlated with the battery temperature to provide the necessary rules for the Fuzzy Knowledge base (*Fig. 11*). The delta_Current is the difference/error between the required charge current and the actual charge current, currently at +0.2A (*Fig. 12*).

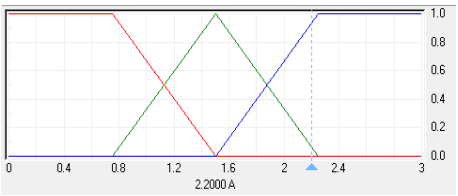

Figure 11. Membership function of the charging current input.

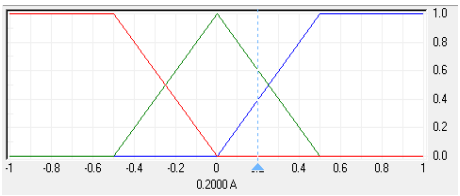

Figure 12. Membership function of the charging current error input.

The Temperature input to the system is the measured battery temperature. Currently 28°C (*Fig. 13*). Finally the membership function of the output variable of the FLCS referring to the digital potentiometer's value is represented in *Fig. 14*.

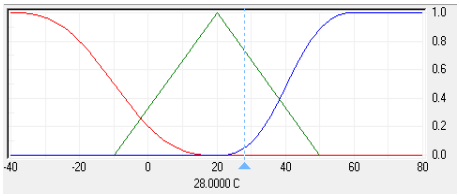

Figure 13: Membership function of the temperature input.

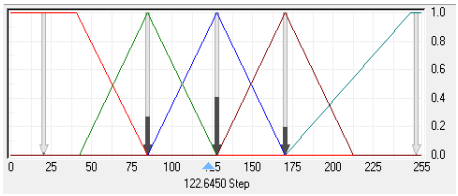

Figure 14: Membership functions of the digital potentiometer output.

We choose to use the Mamdani inference method used for it's simplicity in implementing on an 8 bit microcontroller. The knowledge base was designed using all our experience gained in the field of charging batteries with different chemistries. For defuzzification we chose the Center Of Mass method because it offers more precise calculation of the control signal output at the cost of additional computing power which we were able to deliver to the system by optimizing some other, non time critical algorithm parts, running on the same MCU.

3.4. Running on batteries

When the system is running on battery the cells are carefully monitored and the system enters low power consumption mode when an under-voltage condition is sensed. In order that the UPS enters the low power consumption mode, one of these two conditions must be fulfilled: either the voltage measured on one of the battery cells is less than a predefined threshold or the coulomb

counter is below a predefined value. Both parameters are configurable for flexibility (*Fig. 15*).

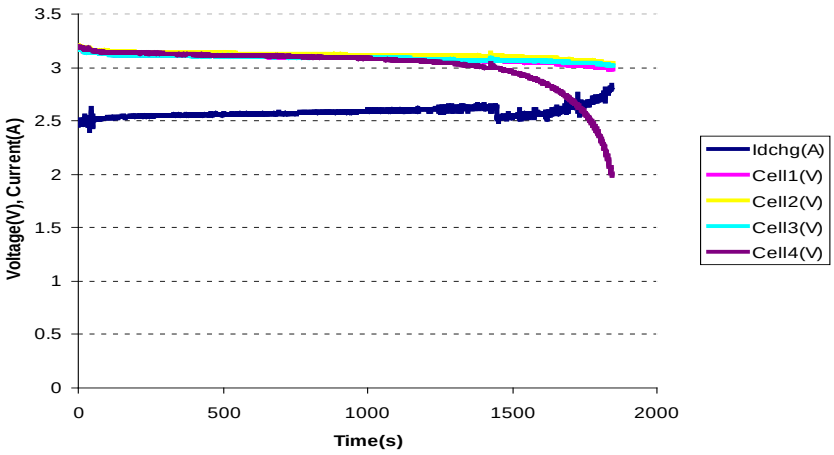

Figure 15: Battery discharge featuring under-voltage protection at 2V/cell.

3.5. The UPS switching technique

In order to keep the system running we need very fast switching between the DC input and the battery sources [16]. For this reason we used a voltage comparator located in the microcontroller. In case the input voltage drops below a predefined threshold the comparator trips, triggering an interrupt in the microcontroller. The interrupt service routine is the highest priority one from all the interrupts used in the system.

The threshold to which the falling voltage is compared is digitally configurable which gives higher flexibility to the system when used in a wide range of input voltage. The switches are composed by P-MOS transistors in back to back configuration for proper blocking [16]. The gate drivers of the switches are designed with active pull-up/pull-down stages to accomplish high speed switching. See the principle of operation presented below in *Fig. 16.*

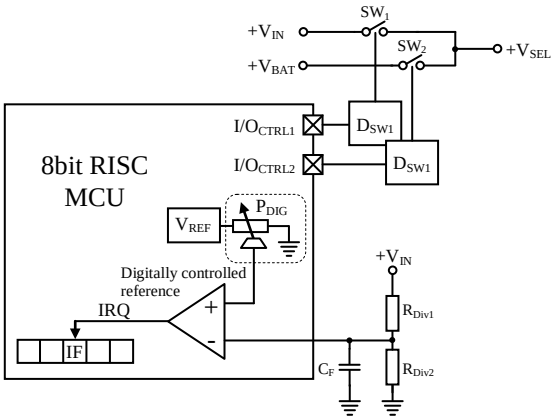

Figure 16: Schematic of the UPS switching technique used.

The delay between the input voltage fall event and the event of switching the current path to the battery is given by the following equation:

$$T_{DELAY} = T_{LPF} + T_{COMP} + T_{IR} + T_{MOS\_close} + T_{MOS\_open} \quad (5)$$

where:

T_{LPF} = Low pass filter to filter out high frequency noise;

T_{COMP} = the response time of the comparator;

T_{IR} = time spent in the interrupt routine;

$T_{MOS\_close=}$ turn off time of the MOSFET connected to the DC voltage input;

T_{MOS_open}= turn on time of the MOSFET connected to the battery.

The longest delay is introduced in this equation by the T_{IR} component. For best results this part of the microcontroller code was optimized for speed by writing this part of the code in assembly language and making this interrupt the highest priority. The measured delay is below 35us, which is sufficient for maintaining the output near close to the reference voltage providing the necessary power to the output.

The high efficiency LTC3780 synchronous buck-boost controller is selected as analog output module because of its very good line transient characteristics. The resulting line transient characteristics of the UPS can be observed in *Fig. 17.*

Figure 17: The line transient effect on 1ms time base.

Channel 1 is the main input voltage (V_{IN}), channel 2 is the main output voltage (V_{OUT}) and channel 3 is the voltage in the common point (V_{SEL}) of the two switches SW1 and SW2, which is also the input voltage in the output buck-boost controller.

The output of the UPS was connected to an electronic load previously set to sink 4A constant current. The UPS is configured to switch on battery if the input voltage falls below 6.2V. The battery configuration used in this setup was made by four of 3.2V LiFePO4 cells connected in series. We can distinguish three different stages from the oscilloscope image.

In the first stage the system is running on the main input, the output voltage is generated from the main input. In the second stage at some point the input voltage falls with dv/dt=3V/ms. As soon as the input voltage drops below the predefined threshold the UPS switches to the battery by connecting it to the buck-boost controller's input.

In the third stage we can see that the output remains stable with damped oscillation around 12V. The ripple voltage amplitude is well below 10% of the +12V nominal voltage, which is defined by the ATX standard validating our system.

3.6. Battery Balancing

As stated in the referenced document [1], in order to accurately balance battery cells, high precision and high resolution measurements of the cells'

voltage are needed. The system is able to measure battery voltages up to 30V with less than 10mV resolution. Most of the mid range microcontrollers have only a 10bit resolution A/D converter on board which was not enough for this purpose. Therefore a stand alone, 12bit, I2C A/D converter has to be chosen [6]. The main idea is presented back in *Fig. 1*. The MCU commands the on board PSU and discharge switches, communicating with the A/D converter via I2C lines. Since the voltage variation on a battery cell is a relatively slow phenomenon low pass filters are used on the analog inputs.

Balancing [2] can be done by passive or active methods. Passive balancing means drawing energy from the most charged cell through discharge resistors. This energy is wasted as heat. Active balancing draws energy from the most charged cell and transfers it to the least charged one. This method presumes less wasted energy, but involves DC-DC converters for each cell and it can be more costly than the previous method. Since the solution presented has to be cheap and the space is constrained, using active balancing is not appropriate.

The faster the balancing the more heat is produced, more space is needed on the PCB since higher power resistors are bigger [10]. On the other hand over-heating the board is not allowed, temperature can also influence the measurements' stability. However temperature compensation is possible since temperature is measured on the board. Balancing 12V/Cell (SLA) batteries versus 3V/Cell (LiFePO4) implies more dissipated heat if using the same discharge resistor [8]. In order to dissipate the same amount of power, PWM controlled balancing is used for each cell of the 12V cells batteries as shown in *Fig. 18a* and *Fig. 18b*.

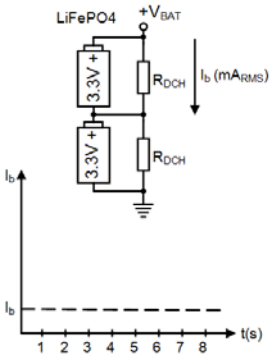

Figure 18a: Direct discharging LiFePO4 Cells.

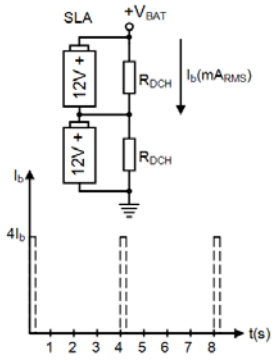

Figure 18b: Slow-PWM discharging SLA Cells.

The balancing algorithm finds the weakest cell, then for each cell calculates the difference between its own voltage and the voltage of the weakest cell (minimum). In case if the cell voltage is less than the discharge limit voltage, discharging is stopped for that cell. This is extremely important to prevent deep discharging [3] of the battery cells [9]. If the difference found is bigger than a preset start value the cell will be discharged. If the difference is less than the differential start value it will be further checked against a preset stop value. If it is less than the stop value the discharging will be stopped for this cell. This algorithm introduces a hysteresis in the balancing procedure. In order to obtain the balancing logic with hysteresis working well, the start voltage parameter needs to be bigger than the stop voltage parameter. The internal impedance of the battery cells can also affect the voltage based balancing if it is done when charging with high current. The best results are achieved if balancing is done near to the end of the charging cycle, when the charging current decreases. The balancing results for six LiFePO4 3.2V/3400mAh cells are shown in *Fig. 19*. The achieved accuracy is self explanatory, presenting a variation between balanced cells comparable to the A/D converter resolution of 8mV/LSB.

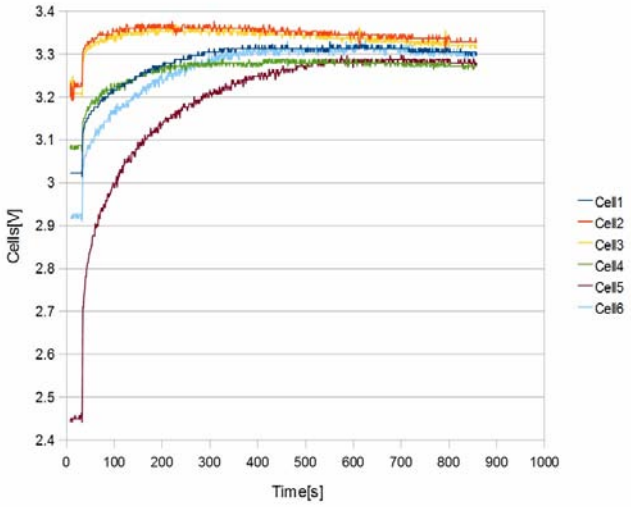

Figure 19: Charge balancing graph of six LiFePO4 cells.

4. Integration of the micro sized UPS

For fulfilling the project's main goal to create an intelligent UPS module, rated near the Top Level of Integration, besides the internal control techniques

and methods an important aspect remains still uncovered in earlier explanations: embedding. Embedding power electronics has some drawbacks regarding the size, wiring, heat dissipation, and communication layers.

4.1. Some physical aspects

In order to facilitate the size related integration aspect in already existing systems the physical dimensions and connection layout of the device were carefully optimized. *Fig. 20* shows the UPS device on the top of a 12V SLA battery for size comparison. It is designed with components on a two sided, multilayer PCB with power components placed on the top, facilitating heat dissipation even in case of passive cooling methods. The digital and analog signal components were placed on the bottom of the PCB, shielded by a GND layer for noise reduction. The three main power component groups, (the charger buck-boost, the output buck-boost and the power switches for current path selecting (marked with red rectangles) were compacted and placed following an optimal topology for high current throughputs. All the wire inputs and outputs were placed in strategically optimal positions to allow short wire harnesses to be used.

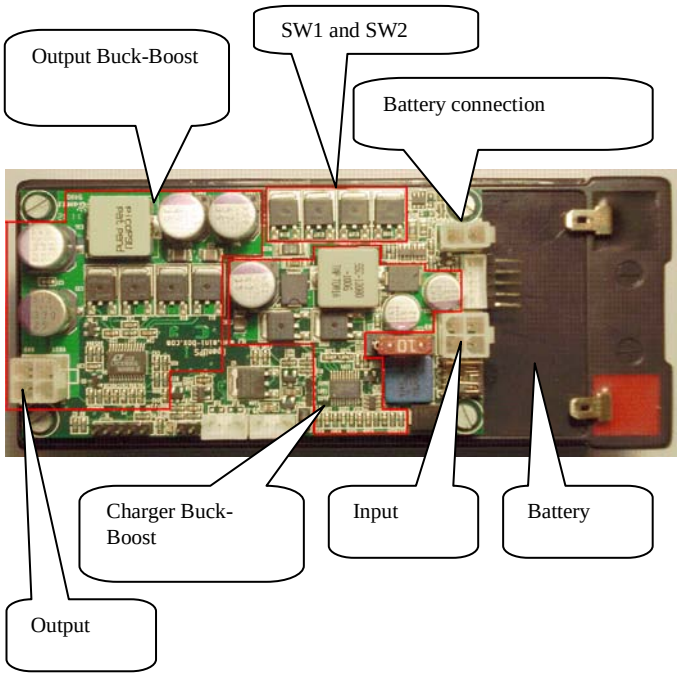

Figure 20: The UPS device, with delimited main functional groups.

4.2. Logical level aspects

On the logical level the UPS can handle two types of integration methods:

- Combined with the battery pack and presented as a SBP (Smart Battery Package) over the SMBUS communication line;
- Like a system level device, usable under various operating systems trough USB line and corresponding low- and user-level drivers.

Both profiles (SMBUS and USB) were integrated in the interfacing algorithm allowing lots of required and even specific (custom) parameters to be set to meet the requirements of the main system.

On the PC side the UPS driver and application software has three main levels upon the lovest hardware level [12]: on the top level is placed the application software presenting a GUI, the lower level consists of the user mode driver and at the bottom of the structure is the HID-USB low level driver (as shown on the right side of *Fig. 21*).

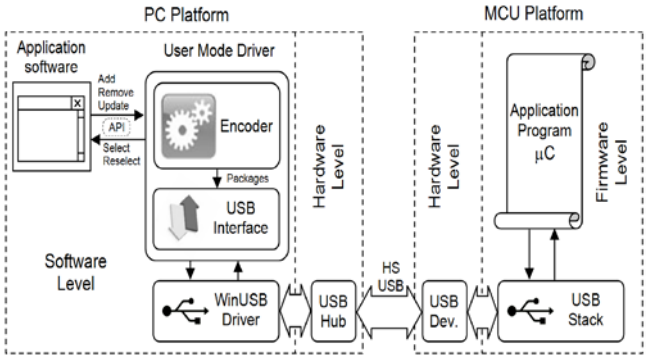

Figure 21: Schematic of the HS USB integration layers.

In the background of the GUI's task another parallel task communicates with the user mode driver via API functions. The user mode driver is also built on level structure [11] as follows:

- the Encoder is responsible for composing the messages and feeding the USB interface. The outcoming messages are packed accordingly to the requests of the communication protocol.
- the USB interface handles the message flow (up and down) between the low level HID-USB driver and the user mode driver.

The universal WinUSB driver is an add-on feature of MS Windows type operating systems since SP2. This low level driver can handle full speed USB

links with a bandwith rated at 40Mb/s, wide enough for handling such applicatons.

On the MCU side an event driven, direct USB Stack has been built over the hardware layer, handling the opened up- and down-pipes of the USB channel (as shown in the left side of *Fig. 21*). The application program runs an advanced parser algorithm to maintain the communication flow as the internal parameter matrix changes over the time. The system is able to send ON/OFF pulse signals to the motherboard based on the Coulomb counter and/or based on the battery voltage level, or based on input voltage level or when starting. Even more, once connected to a PC, the device installs itself as a smart battery in Windows operating system, using the Windows HID-USB driver without the need of any additional driver installation, and becomes immediately visible as a battery icon in the tray bar. Features include both UPS and LAPTOP mode.

4.3. Special and proprietary features

Many of today's UPS applications are situated in a price sensitive field where the possibilities of integration, and feature palette are both often minimized or even non existent to preserve a low price range. As stated before the UPS developed by us tries to overcome these limitations with a wide palette of special and proprietary features. First it can handle different types of batteries; many types of UPS are limited to a predefined battery type. It also has a Battery Wizard application aiding the user in setting some entry level parameters to the device selecting between only a few predefined battery profiles. The user resumes selecting the battery type and capacity, the nominal battery voltage and the number of battery cells to use. In addition individual or global measuring points are defined with graphical representation on the right side of the GUI, aiding the user to properly connect the individual measuring points to the battery poles. Then the wizard generates the charging voltages, charging currents, as well as initial voltage based remaining capacity estimation (fuel gauge) thresholds, under-voltage shutdown threshold and other useful parameters (*Fig. 22*). Besides of the wizard application the user also has the ability to manually change each of the generated parameters to further customization.

Another feature consists in an increased flexibility for fuel gauge estimation, where the voltage based thresholds are also configurable. There are six estimated parameters, each of them setting a threshold for 0%, 10%, 25%, 50%, 75%, 100% fuel gauge, used by the MCU firmware to determinate the initial, remaining battery run-time.

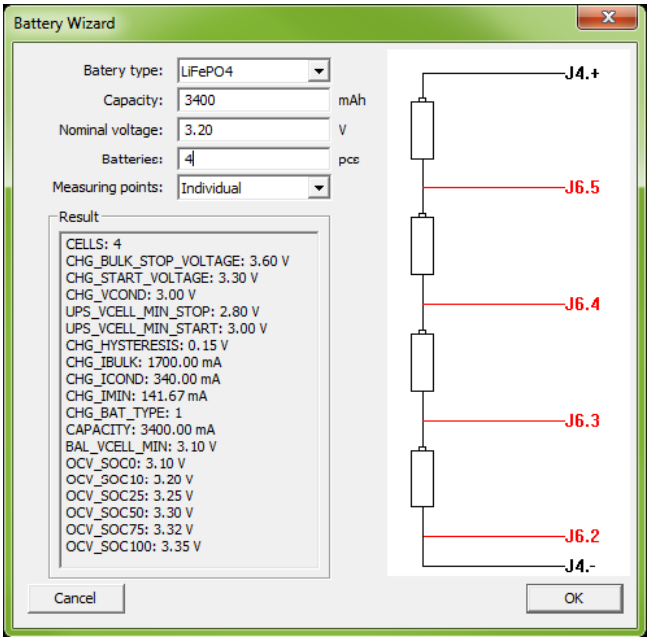

Figure 22: Screenshot of the Battery Wizard GUI.

When the system is running on battery and its voltage falls below the predefined under-voltage threshold or the coulomb counter is down to a minimal value the UPS takes care to shut down the OS and PC nicely, preventing OS damages. After the system has shut down, the device achieves ultra low power consumption (below 50uA) to preserve battery. This feature is achieved with a proprietary MCU power supervisor circuit disconnecting the 3.3V rail which also powers the MCU and other digital logic ICs. In case of a discharged battery the UPS can be waked up only if the input voltage appears in which case the battery re-charging is started immediately. In case of a partially charged battery the UPS can be woken up also by pressing its start button.

5. Conclusion

More time spent on this project means being more involved in low level optimization of the control algorithms. The system was designed to provide user specified regulated voltage output over a wide range of input voltages, battery backup, multi-chemistry charging and cell balancing by means of a single PCB at a noticeable level of efficiency (over 80%), all controlled by a single mid-range MCU.

Any input, output and charge voltage between 5-30V can be used in any possible combination. This allows the system to be easily embedded in many existing electrical systems. Features also include USB and SMBUS interface, programmable parameters and thresholds, multiple battery chemistry, battery balancing up to 6 cells, Coulomb counting.

At the end of this paper it can be concluded that the main goals can be considered fulfilled at a relatively low cost, where the optimum between price, system integration skills and power efficiency have been achieved for a relatively wide application palette for these types of devices.

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