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A New Model of Dynamic Logic Circuit with NMOS based Keeper

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Abstract: Dynamic logic circuits are widely popular due to a smaller number of transistors and consume less area. But the time to switch between logics is higher due to higher contention value. A new model of the logic using nMOS based keeper circuit is proposed and the performance is evaluated using Cadence tools. Comparative results demonstrate the suitability and competency of the proposed circuit.

Keywords: Keeper circuit, dynamic node, nMOS based keeper.

1. Introduction

High speed and low power logic circuit designs are more significant in VLSI design [1], [2]. Dynamic logic circuit needs to have almost half the number of transistors compared to traditional logic circuits. It saves better power than traditional logic circuits. Dynamic logic consists of a precharge device, a pull-down network, pMOS keeper and a footer device. A clock signal is used to control and operate domino logic.

Basically, dynamic logic circuits operate in two phases, these are precharge phase and evaluation phase. When clock is high it is called evaluation phase and when the clock is low it's called precharge phase. However, the main drawback of domino logic circuit is that it is not always connected to V_{DD}. A keeper device has been used to compensate that. When all inputs are high then the stored voltage at the dynamic node should be removed through the PDN (Pull Down Network). That produces some time delay between the conduction of keeper transistor and pull down network. Also, that causes increasing time delay, power consumption and noise sensitivity [3]. To minimize these

drawbacks, we need to design a new keeper architecture which gives better performance.

A new architecture is proposed in this research for better performance in terms of power consumption and noise margin of dynamic logic. The power consumption of logic circuits is calculated [3] by

$$P_{avg/gate} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

Here, the power consumption of the logic gates by charging/ discharging of circuit capacitances is denoted by $P_{switching}$. Short circuit current flowing from V_{DD} to ground is denoted by $P_{short\text{-}circuit}$ during output voltage alterations.
Leakage power ($P_{leakage}$) is dramatically changed by scaling down the technology and enhanced by temperature, which is very significant for the reduction of leakage power of dynamic logic circuits.

The proposed nMOS based resistive keeper circuit is employed for simulating 4, 8, 16, 32-input OR gates, by using Cadence Virtuoso tool. The obtained results demonstrated the enhanced noise tolerance, reduced power dissipation and time delay as compared to conventional logic circuits.

Recently proposed [4]-[15] dynamic logic circuits are presented in *Section 2*. *Section 3* describes the proposed resistive keeper circuit. *Section 4* presents the proposed model with different combinations in the pull down network. *Section 5* depicts the analysis and simulation results of the proposed technique. Finally, the paper concludes in *Section 6*.

2. Existing Works

The easiest way to improve the noise tolerance of dynamic logic circuits is to provide a weak keeper device to maintain the required amount of charge in the dynamic node. The gate of a keeper transistor is connected to the ground as used in some [4] domino logic, where the keeper device is always ON. But this type of design consumes more power as DC power continuously follows through that keeper transistor. To compensate that problem, a feedback keeper transistor is designed [4]. This model controls the keeper device during the evaluation phase as shown in *Fig. 1*. The main purpose of the keeper device is to reduce the contention time in the evaluation phase, when the pull down network is ON. So, a keeper circuit should be designed to reduce the leakage current through pull down network for wide fan-in gates.

Several research groups [4] - [15] have proposed different versions of the strong keeper circuit model, which minimize the contention problem. Those models make the keeper device inactive during the switching time and are better for noise tolerance in the dynamic logic circuits. However, these models are

unable to reduce the leakage current to a tolerable level. For that reason, the dynamic node cannot protect itself during PDN switching.

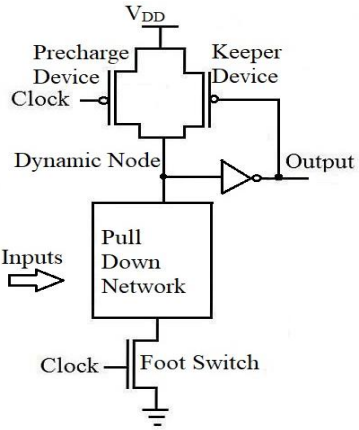

Figure 1: Traditional domino logic

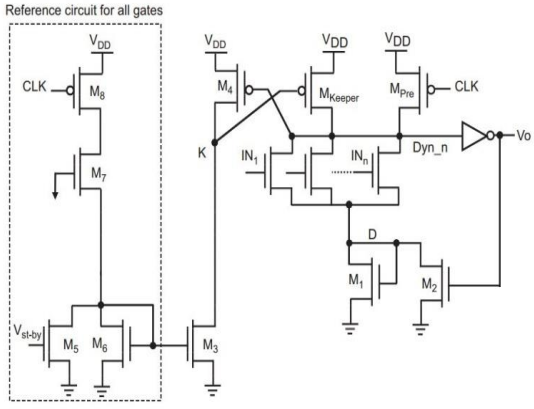

Figure 2: Controlled keeper by current comparison domino circuit (CKCCD) [5]

Ali et al. [5] designed a reference circuit to sense the PDN leakage current. Depending of the amount of leakage current of dynamic node, a mirror current is generated, which is responsible to control the gate of the keeper device. This design contains a large number of transistors as compared with other circuits as shown in *Fig.* 2.

Conditional keeper domino logic is one of the popular domino logic which is presented by A. Alvandpour et al. [6]. Two keeper transistors (weak and strong)

are employed in this technique. These extra transistors increase the cell area and can improve the noise immunity, although, the circuit consumes significant power.

In high speed domino circuits, several inverters are used to control the current flow through the pMOS and nMOS network at the beginning of the evaluation phase [7]. This technique has induced the need for a larger pMOS keeper transistor. In this model, current flow of the pMOS and nMOS keeper transistor network is controlled by two-time delay inverters. However, their circuit was unable to provide sufficient protection against the internal noise at the dynamic node.

Dadgour and Banerjee et. al. [8] presented a new keeper architecture where they reduced the contention current and power consumption to improve the performance of dynamic logic. There are several components in their model such as: two keeper devices, variation coupled keeper (VCK) etc. But their model shows lower noise margin because of leakage current affected the dynamic node.

Current Comparison Domino (CCD) is another technique to compensate the leakage current of domino logic [9]. This technique is used to control a pull-up network instead of a pull down network. A reference circuit is used to provide the proper output by comparing the current between reference circuit and pull up network. This technique is efficient but it needs more overhead area compared to conventional domino logic circuits.

Diode footed domino (DFD) circuits [10] produce better results in terms of noise immunity and leakage current. In this design, an nMOS is connected with the PDN and called as diode footer transistor. This footer transistor reduces the leakage current, which is generated due to stacking effect. However, more area overhead and power consumption are the significant drawbacks of this presented model.

Asyaei et al. [11] designed a sense amplifier to generate proper voltage on the output node. There are two stages of their model: one is pull down network designed with variable inputs of logic gate and the other is the sense amplifier which sensed the voltage difference between the point A and B as shown in *Fig. 3*. Basically, the dynamic node of this circuit is controlled by these two points. It reduces the leakage current due to the stacking effect whereas needs a larger number of transistors and consumes more power.

A new model with an external circuitry is proposed by Lih et al. [12]. The additional circuit controls the conductance of the keeper transistor by generating the replicate leakage current of the PDN (pull down network) as shown in *Fig. 4.* The keeper circuit is controlled by dynamic node leakage current, which is also generated by an external circuit. This model also used two keeper transistors and extra circuits which increased the overhead area.

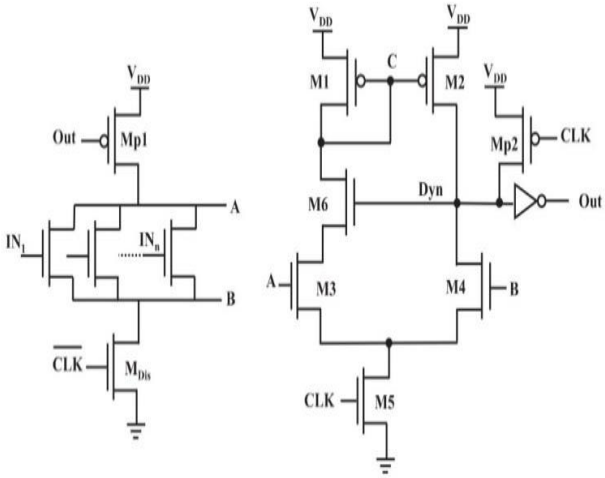

Figure 3: VCD circuit [11]

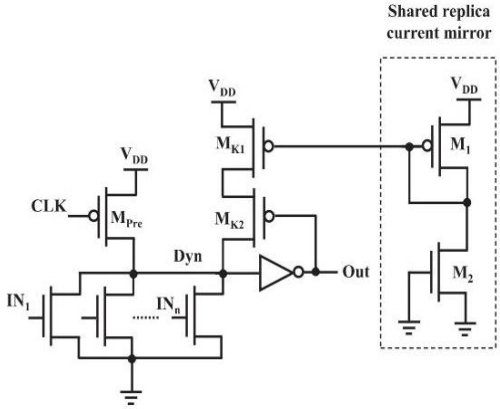

Figure 4: LCR keeper Circuit [12]

However, in this research, two nMOS based resistive keeper models are presented. The circuits control the gate to source voltage of keeper device with differential waveforms to enhance the noise tolerance of the dynamic logic circuits and lower leakage power consumption.

3. Proposed Design

The proposed circuit controls the gate of the keeper device with differential waveforms. This gate is designed by using two nMOS transistors (T_{R1} and T_{R2}). These transistors are connected in parallel but are not operated at the same time. Both nMOS transistors are designed with different length and width. When any small amount of leakage current passes through PDN or any path, it tends to be grounded. At that time, T_{R1} operates and controls the gate of keeper device to maintain the proper state of the dynamic node. This happens according to $I_{TR1}= I_X-I_{leakage}$, $I_{Tp}= I_{DD}- I_{TR1}$, whereas I_X is dynamic node current and $I_{leakage}$ is the leakage current. The inverter is operated to supply the proper voltage on the gate of the keeper device. Any current flowing in the dynamic node while the pull down network is in logical OFF mode is considered as leakage current ($I_{leakage}$).

Transistor T_{R2} is connected in parallel with T_{R1}. When the pull-down network conducts T_{R2} operates and controls the gate of the keeper device. Besides, when all inputs of the pull down network become low, a small amount of leakage current is flowing. For that reason, a footer switch is added to reduce the leakage power.

This leakage current also decreases the noise tolerance and increases the robustness of the circuit. As we know, a parasitic capacitance is induced in the dynamic node at the beginning of the evaluation phase which provides more time delay in the dynamic logic. The feedback of the nMOS based resistive circuit can control the gate of the keeper device by applying different waveforms. Conventional dynamic logic circuits produce contention between pull down network and keeper device. That increases the leakage current, time delay and power consumption. But the proposed work decreases this problem between the PDN and keeper device contention evaluation phase.

Also, T_w can be keeping the contribution of sub threshold leakage reduction due to the stacking effect in the evaluation phase [13]. So, the leakage power of this circuit is reduced by applying these techniques. In the dynamic logic circuit, the size of the keeper device can be minimal because the leakage current of the pull-down network is very low. Also, more than 32 input OR gates give better noise immunity if the keeper sizes are increased. However, the proposed circuit reduces the ratio of W_k / W_p.

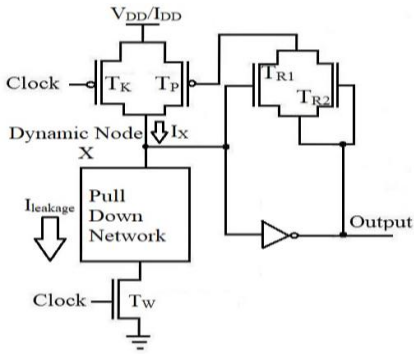

Figure 5: Proposed dynamic logic

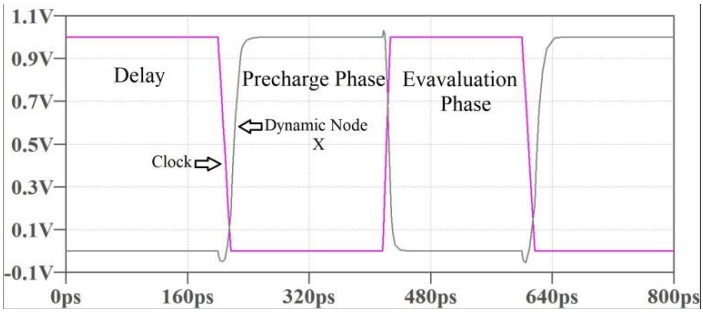

Figure 6: Waveshape of clock versus dynamic node voltage

3.1 Precharge Phase

As shown in *Fig. 5*, when the clock is low, precharge transistor T_k turns ON and footer transistor T_w turns OFF. At that time the dynamic node charges to V_{DD} and the output logic is '0'. At this time T_{R2} is OFF and T_{R1} is in ON state. The gate-source voltage of the keeper device is controlled by the feedback of resistive gate. In this phase, leakage current is reduced due to stacking effect.

3.2 Evaluation Phase

In this phase, the precharge device turns OFF and footer switch (T_W) turns ON.

A. Inequality:

If at least two inputs differ in case of the OR gate, one leg of the pull down network conducts to discharge the dynamic node via T_W. At this time, transistor T_{R1} turns OFF and T_{R2} is controlled by the inverter output voltage. Basically,

the keeper circuit works as a gate for the keeper transistor T_p. Operation of T_p is dependent on differential waveforms of the proposed keeper circuit. The feedback of nMOS based keeper circuit maintains sufficient voltage to control the logic value in the dynamic node, X. Keeper circuit is always controlled by the dynamic node voltage and at least one nMOS is ON in every logic combination. The dynamic node wave shape is shown in *Fig. 6.*

B. Equality:

When all inputs are high in the evaluation phase, foot switch (T_W) is ON which makes a discharging path for the dynamic node and T_{R2} produces the inverter voltage to control the keeper device as shown in *Fig. 7*. A contention time occurs between the nMOS network and keeper device because the keeper device is ON until the inverter voltage goes to minimum to turn off the keeper device in conventional dynamic logic. However, this problem is minimized with this work.

Table 1: Size of transistors for different inputs of OR gates

Wide Fan	4	8	16	32
$(W/L)_{TK}$	3Lmin/ 1Lmin	3Lmin/ 1Lmin	3Lmin/ 1Lmin	3Lmin/ 1Lmin
W_{TW}	8Lmin	8Lmin	8Lmin	11Lmin
$(W/L)_{TR1}$	3Lmin/ 5Lmin	3Lmin/ 5Lmin	3Lmin/ 6Lmin	3Lmin/ 6Lmin
$(W/L)_{TR2}$	3Lmin/ 6Lmin	3Lmin/ 6Lmin	3Lmin/ 6Lmin	3Lmin/ 6Lmin
$(Wp)_{Inverter}$	6Lmin	6Lmin	6Lmin	6Lmin
$(Wn)_{Inverter}$	6Lmin	6Lmin	8Lmin	8Lmin
$(W/L)_{TP}$	3Lmin/ 5Lmin	3Lmin/ 5Lmin	3Lmin/ 5Lmin	3Lmin/ 6Lmin

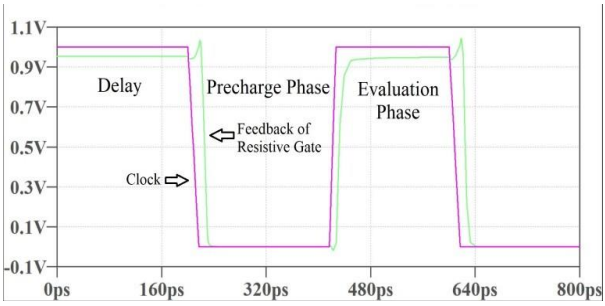

Figure 7: Clock versus feedback resistive gate

4. Sizing of Transistors

In this research, several works have been studied to be compared with the proposed circuit such as: high-speed domino circuit (HSD), the controlled keeper by current comparison technique (CKCCD) (*Fig. 2*), voltage comparison-based domino logic circuit (VCD) (*Fig. 3*) and the proposed dynamic logic circuit. In HSD circuit, different widths to length ratios are used to get the best performance. In conditional keeper domino logic (CKD), length is used as 2Lmin.

We used OR4, OR8, OR16, OR32 gates and time delay are taken as 170ps, 190ps, 200ps and 210ps. It is to be noted that the size of the transistors are adjusted to obtain the best result as shown in *Table 1*. Weak and strong keepers are used and varied to get the desired result. An inverter is used, which has the width to length ratio of 2.

In the proposed technique, T_P is the keeper transistor which compensates the leakage current and increases the robustness of the circuit. As we know, upsizing the keeper transistor increases the noise immunity but also increases the power consumption. So, a minimum size is required to increase the noise tolerance and size of keeper transistor should be lowered to avoid the flow of leakage current. Transistor T_w is inserted to avoid the unwanted discharging path in the dynamic node due to leakage current. Also, the length of this transistor is increased to reduce the leakage current flowing and power consumption. In the proposed resistive gate circuit, the size of two transistors must be asymmetric to generate the proper voltage to control the gate of keeper device. The length of the transistor is upsized followed by different OR gates. *Table 1*. shows the size of transistors with different inputs of OR gate. In the pull down network, all nMOS transistors are of the same width where, 22 nm transistors are used and the width is set to minimum W= 3Lmin.

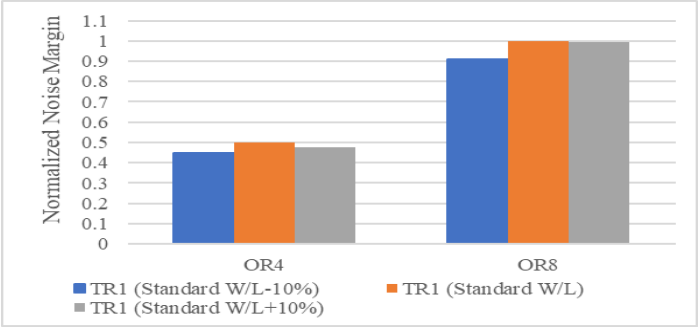

Figure 8: Noise tolerances for various W/L ratios of transistor TR1

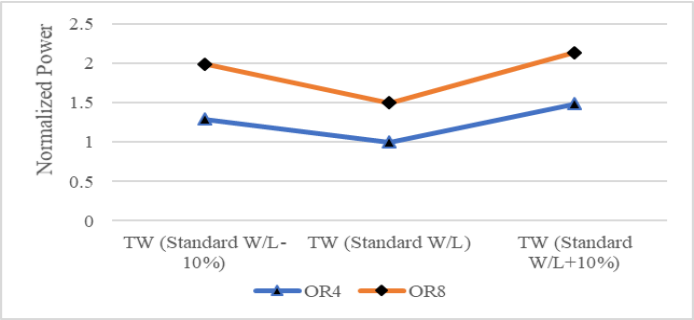

Figure 9: Power consumption for various W/L ratios of transistor Tw

The W/L ratio of T_{R1} is set from 3L/5L to 3L/6L for wide fan-in OR gate in order to get better noise immunity. By changing that ratio from "standard W/L-10%" to "standard W/L+10%", obtained noise tolerances are shown in *Fig. 8*. So, these standard ratios are chosen to operate the resistive gate. Selected standard W/L ratio of T_w for low power consumption is shown in *Fig. 9*. Basically, T_w can contribute to decrease the leakage current flowing at evaluation phase. So that, proper sizing of this type of transistor provides better noise tolerance and low power consumption.

5. Simulation Results

Simulation experiments were carried out using the LTspice simulation tool with 22nm PTM technology model [14]. Generated wave shape and data are taken from wide fan-in (4, 8, 16, 32 input) OR gates and the results are compared with several previous works. It is clearly noticed that the proposed model provides better noise tolerance. These data are obtained by setting (W/L) T_K = (3L/ 1L) min, (W/ L) T_p= (3L/ 5L) min and W_p= 6L min, W_n= 6L min for output inverter.

5.1 Noise Margin Analysis

Noise margin is defined as the rate of stability of a circuit and noise tolerance of stored data at the dynamic node. Leakage measurement method can explain the Unity Noise Gain (UNG). Where different types of identical noise pulses are applied on inputs and amplitudes of output noise are analyzed. Basically, UNG is used for making the comparison between leakage and noise robustness of domino logic circuit and it can be estimated [15] by using the following equation:

$$UNG = \{V_{in}; V_{noise} = V_{out}\} \tag{2}$$

In the proposed dynamic logic circuit, when the circuit is affected by noise, the keeper device will not work perfectly because the generated noise could modify the gate voltage of the keeper device. For that reason, two-external voltages are applied on the keeper device with opposite polarities. The gate of the keeper device is connected with an external noise source and the drain or dynamic node is connected with another external noise source. A dynamic circuit is considered to be good when the designed circuit can tolerate more noises without data distortion.

It is noticeable that the noise margin (NM) is decreased with the number of inputs as shown in *Table 2*. So, the fact is that the number of inputs is a significant factor. The noise tolerance values of the proposed model give better normalized data.

Table 2: Normalized noise margin (NM) and power (NP) of different OR gates

Different Models	Fan-in 4		Fan-in 8		Fan-in 16		Fan-in 32	
	NM	NP	NM	NP	NM	NP	NM	NP
HSD [7]	0.37	2.03	0.33	1.94	0.3	1.68	0.27	1.81
VCD [8]	0.36	2.4	0.32	2.2	0.28	1.9	0.26	1.8
CCD [9]	0.36	1.32	0.34	1.3	0.32	1.31	0.29	1.24
Proposed	**0.395**	**1**	**0.379**	**1**	**0.361**	**1**	**0.340**	**1**

5.2 Power Analysis

Table 2 shows the comparison of power consumption. This data is normalized with respect to the proposed circuit. All data was taken using 22nm Predictive technology model. The proposed circuit shows a significantly lower amount of power consumption as compared with the high-speed domino (HSD) logic and Voltage control domino circuit (VCD). In the collection of high speed domino (HSD) logic data, a change of the size of the keeper device is required.

In the current comparison domino circuit, several models are used to control the gate of the pMOS keeper device which increases the time delay. However, the proposed circuit reduces the time delay using nMOS based resistive gate.

The normalized power (NP), delay (ND) and noise margin (NNM) are shown in *Fig. 10*. The figure shows, that a better decrement of power and delay is achieved in the 22nm model while the noise margin gets better value in the 45nm model. *Table 3* presents the standby power of the proposed circuit showing lower power consumption in OR32 and OR16 and also shows higher power consumption rate than the model proposed in [21] for 8 inputs OR gates.

Table 3: Comparison of standby power consumption in μW

Models	CCD [9]	CKCCD [10]	Proposed
OR8	1.5	1.6	***1.7***
OR16	1.8	1.6	***1.5***
OR32	1.7	1.6	***1.4***

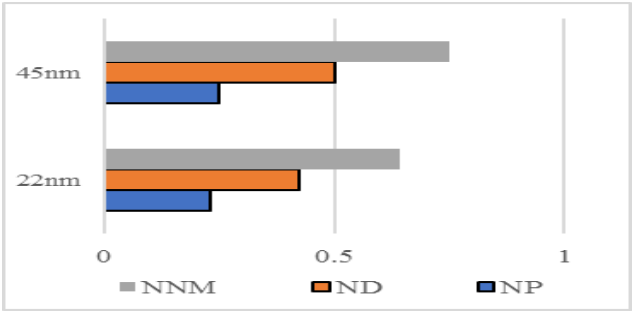

Figure 10: Normalized data for several aspects of measurement

5.3 Area Calculation

The layout of the proposed model is designed using Cadence Virtuoso tool and checked by DRC)Design Rule Checker(and LVS)Layout versus Schematic). The proposed techniques have been compared with several conventional methods. The proposed model required only 39 transistors for designing the 32 inputs OR gate while the other techniques need more transistors as shown in *Table 4*. Also, area overhead data obtained by using 90 nm technology is shown. The proposed circuit designed at 90nm technology requires an area of 8.1055 μm^2,whereas the same circuit designed at 45nm technology (*Fig. 11*.) requires only 2.2385 μm^2.

Table 4: Comparison of the number of transistors with other works for 32 inputs of OR gate and area overhead using Cadence Virtuoso tool for 2 inputs of OR gate using 90 nm model.

Several Works	Number of Transistor	Area
CKCCD [10]	42	18.250 μm^2
LCR [12]	37	10.1875 μm^2
CCD [9]	41	14.9062 μm^2
Proposed	***39***	***8.1055 μm²***

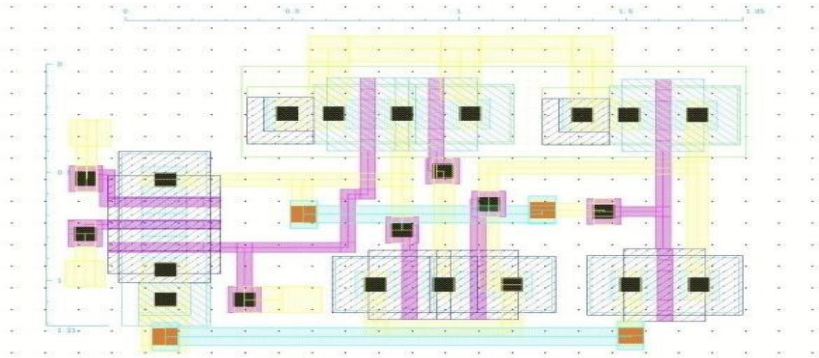

Figure 11: Layout of the proposed circuit using 45nm model

6. Conclusion

A keeper circuit consisting of only two nMOS transistors has been designed for a dynamic logic circuit. The proposed circuit acts like a resistive gate for the keeper transistor. As this circuit is connected in series with the gate of the keeper transistor, so the current through the resistive circuit is less and makes the keeper weaker at the start of the operation. The contention time is reduced as needed. Extensive simulation results demonstrate that the proposed circuit consumes less power and provides better noise margin as compared with several conventional models.

References

[1] Anders, M., Mathew, S., Bloechel, B., Thomson, S., Krishnamurthy, R., Soumyanath, K., and Borkar, S. Y., "A 6.5 GHz 130 nm single-ended dynamic ALU and instruction scheduler loop", *in Proc. ISSCC Dig. Tech..*, pp. 410–411, 2002.

[2] Kuroda, T., Fujita, T., Mita, S., and Nagamatsu, T., "A 0.9 V 150 MHz 10 mW 4 mm/sup 2/2-D discrete cosine transform core processor with variable-threshold-voltage scheme", *IEEE Solid-State Circuits Conference. Digest of Technical. 42nd ISSCC*, 1996, pp. 166-167.

[3] Rabaey, J. M., Chandrakasan, A. P., and Nikolic, B., "Digital integrated circuits. Vol. 2." Englewood Cliffs: Prentice Hall, 2002.

[4] Alvandpour, A., Krishnamurthy, R., K. Soumyanath, and Borkar, S. Y., "A conditional keeper technique for sub-0.13/spl mu/ wide dynamic gates", in *Proc. Int. Symp on VLSI Circuits. Digest of Technical*, 2001, pp. 29–30.

[5] Peiravi, A., and Asyaei, M., "Robust low leakage-controlled keeper by current-comparison domino for wide fan-in gates", *Integration, the VLSI journal*, vol. 45, no. 1, pp. 22-32, Jan. 2012.

[6] Alvandpour, A., Krishnamurthy, R. K., Soumyanath, K., Borkar, S. Y., "A sub-130-nm conditional-keeper technique", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 633–638, May. 2002.

[7] Anis, M. H., Allam, M. W., Elmasry, M. I., "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.10, no. 2, pp. 71–78, Aug 2002.

[8] Dadgour, H. F., and Banerjee, K., "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic OR gates", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no.11, pp. 1567-1577, Oct. 2009.

[9] Peiravi, A., and Asyaei, M., "Current-comparison-based domino: New low-leakage high-speed domino circuit for wide fan-in gates", *IEEE transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 21, no. 5, pp. 934-943, May. 2013.

[10] Mahmoodi-Meimand, H., and Roy, K., "A leakage-tolerant high fan-in dynamic circuit design style", in *Proc. of the IEEE International Systems-on-Chip (SOC) Conference*, 2003, pp. 117–120.

[11] Asyaei, M., "A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep sub-micron technology", *I*ntegration, *the VLSI journal*, vol. 51, pp. 61-71, Sept. 2015.

[12] Lih, Y., Tzartzanis, N., and Walker, W. W., "A leakage current replica keeper for dynamic circuits", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 48-55, Jan. 2007.

[13] Kim, C. H., Roy, K., Hsu, S., Krishnamurthy, R., and Borkar, S. Y., "A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits", *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 14, no. 6, pp. 646–649, July. 2006.

[14] Predictive Technology Model (PTM), The 22-nm High Performance V2.1 Technology of PTM Model. Available online: /http://ptm.asu.edu/model card/HP/22 nm_HP.pm.> 2008.

[15] Ding, Li., and Mazumder, P., "On circuit techniques to improve noise immunity of CMOS dynamic logic", *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 12, no. 9, pp. 910-925, Sept. 2004.

[16] Islam, R., and Biswas, S. N., "A low power dynamic logic with nMOS based resistive keeper circuit", IEEE *International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)*, 2017, pp. 181-185.